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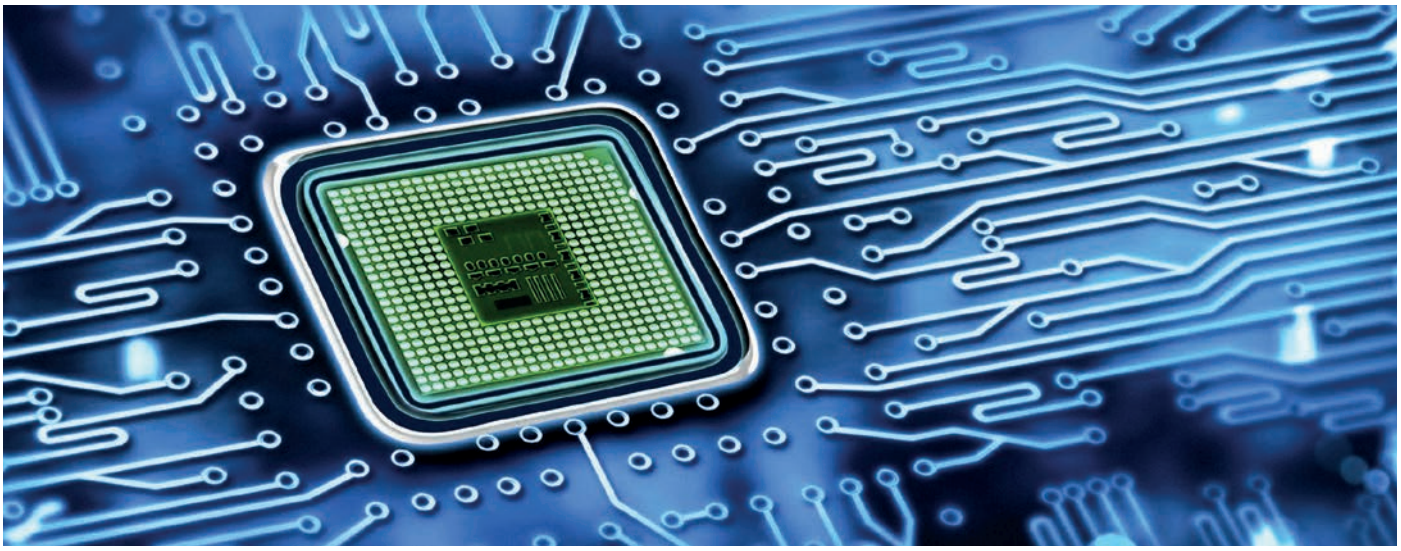

Testing customizable computer circuits with unused memory blocks can improve fault detection and lower the strain on system resources.

Microchip design

Better built-in fault detection

A more effective way of testing integrated circuits can help manufacturers of digital devices improve reliability

A new 'built-in self-test' (BIST) computer architecture that offers better fault detection for custom-built circuits while using fewer system resources has been developed by researchers at Japan's NAIST[1]. The architecture enhances the safety and reliability of highly complex, made-to-order devices, such as medical electronics or optical transmission networks.

Field-programmable gate arrays (FPGAs) are a modern type of computer chip based around a series of programmable components known as 'logic blocks'. Device designers configure and wire the FPGA logic blocks to meet their needs, instead of ordering traditional application-specific integrated circuits (ASICs) from chip manufacturers. This flexibility, which can cut development costs and shorten times-to-delivery, has currently given FPGAs a US$4 billion slice of the lucrative semiconductor market.

Monitoring FPGAs for defects, such as transistor ageing, however, is problematic. ASIC-type chips have built-in tests, known as scan-based BISTs, which send pseudo-random data patterns through a series of 'flip-flop' circuits that can switch between one of two bi-stable states. By comparing the observed data signature with the expected results, this method can identify performance degradations or manufacturing defects. Unfortunately, FPGAs do not have built-in 'scan chains' that shift in and shift out the testing data from the primary microchip design. Instead, redundancies have to be introduced that use the chips' logic elements — a situation that can tax up to 50 per cent of a system's resources.

Tomokazu Yoneda, Michiko Inoue and colleagues at NAIST's Dependable System Laboratory discovered that self-testing with on-chip memories could lessen the load on FPGA logic elements. They configured unused memory blocks to run 'shift register' circuits that use clock signals to shift in or shift out data. Then, they carefully designed a way to insert the shift registers as 'test points' into computer architectures to maximise FPGA reliability.

When the team tested their concept with experimental circuits, they found a remarkable difference in delay test quality — a 5 to 6 per cent boost in fault detection compared to previous methods. "Test point insertion is a key factor in improved fault coverage," explains Yoneda. "Our method can find more resources and insert more test points, since it utilizes unused memory blocks."

Because memory blocks are inherent components of FPGA users, the new self-test design can be easily integrated into current chip design flows and produce significant savings. "Current dual- and triple-mode redundancy solutions for products that require high field reliability are not cost effective," says Yoneda. "This work is promising since it can provide high reliability without any redundancy."

Reference

1. Ito, K., Yoneda, T., Yamato, Y., Hatayama, K. & Inoue, M. Memory block based scan-BIST architecture for application-dependent FPGA testing. *FPGA '14 Proceedings of the 2014 ACM/SIGDA International Symposium on Field-programmable Gate Arrays* 85–88 (2014).

More information about the group's research can be found at the Dependable System Laboratory webpage:
http://dslab.naist.jp/index-e.html