NAIST® Research Highlights

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Computer engineering

More tolerance, less waste

Microchip fault tolerance that consumes one-third less power may now be possible with new chip design

Modern microprocessors contain billions of transistors that have small capacitances (ability to store electrical charge) and low supply voltages. These properties make them prone to failure since they are vulnerable to background noise, cosmic radiation and environmental vibrations. Engineers can improve the reliability of a microprocessor by incorporating extra copies (or redundancies) of critical components in the system, so that when one component fails, another takes over.

However, conventional redundancy architectures, such as the triple modular redundancy (TMR), have all their components — including redundancies — hard-wired into the circuit. Consequently, the lifespan of devices is limited by their least reliable unit.

Now, Jun Yao, Yasuhiko Nakashima and colleagues at NAIST have proposed a low-cost redundancy architecture called Explicit Redundancy Linear Array (EReLA), which offers greater flexibility and better automation than conventional architectures[1]. Processors based on this novel design offer the same functionality, consume less power and have ten times longer lifetimes than conventional processors.

TMR has been the preferred architecture because it comes with configurable isolation (between input, output and power) and hot swap technologies (which allow systems to be switched without shutting down); the former enables defective components, or failures, to be detected and isolated, while the latter ensures smooth running of the system when a fault occurs.

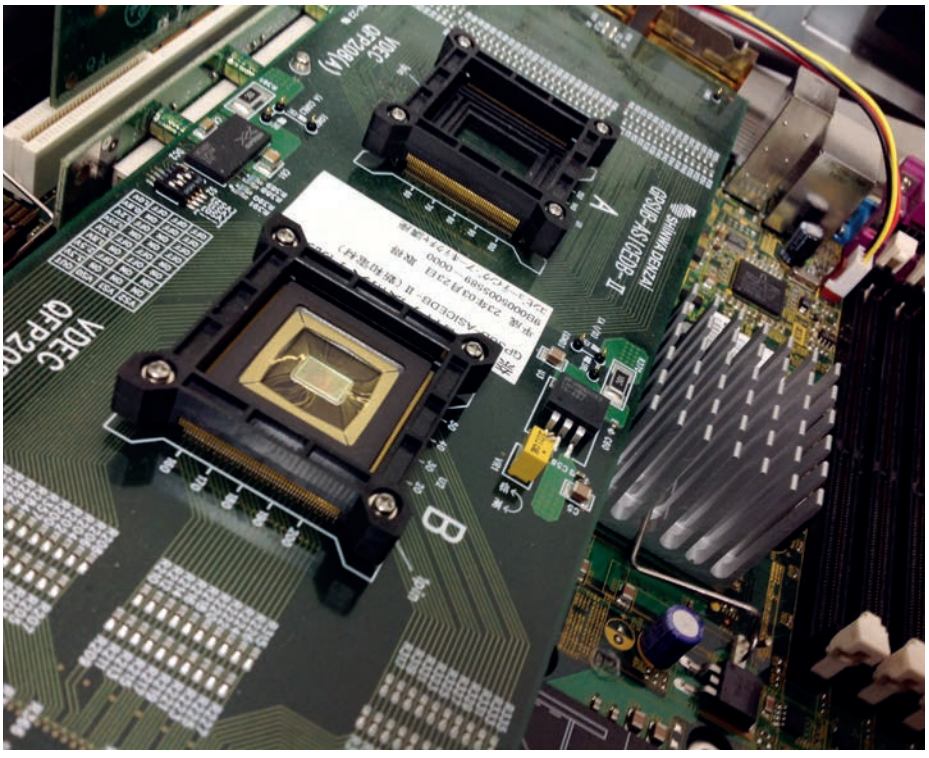
> **“The EReLA architecture provides a cost-effective way to maintain the growth in computer performance for the future.”**

The researchers have incorporated two novel features in the design of EReLA: a fully automated method for locating failures in the system and a self-tuning mechanism that simplifies the hardware needed for diagnosis. To locate permanent failures in TMR, triple redundancies and voter logic are used: three systems perform a function and the result is processed by a majority-voting system to produce a single output — costing both time and money. The newly proposed EReLA does not require either.

“The EReLA can detect erroneous units by itself,” says Nakashima. “It comes with an ‘approximate computing mode’ that can tolerate errors in non-important computations.”

The researchers have built a prototype chip based on EReLA (see figure) and showed that its fault tolerance — a measure of how well the system performs in a failure — is similar to those based on TMR. In addition, the power consumption is reduced by a third due to the simpler hardware. These findings are significant for miniaturizing devices and developing low-cost, low-power, highly reliable computers.

“The mean time between failures of high-end computers is becoming shorter and shorter,” says Nakashima. “The EReLA architecture provides a cost-effective way to maintain the growth in computer performance for the future.”



The new EReLA architecture offers a cost-effective, lower-energy-consumption method to boost computer performance.

Reference

1. Yao, J., Nakashima, Y., Saito, M., Hazama, Y. & Yamanaka, R. A flexible, self-tuning, fault-tolerant functional unit array processor. *IEEE Micro* **34,** 54–63 (2014).

More information about the group’s research can be found at the Computing Architecture Laboratory webpage:
http://arch.naist.jp/index-e.html